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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/695,408
Filing Date: October 28, 2003
Appellant(s): RANGAN ET AL.

Brocade Communications Systems, Inc
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/24/2008 appealing from the Office action mailed 9/20/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Patent Application Publication 2003/0140210 A1 Testardi 07-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Testardi (Pub #2003/0140210).

Regarding independent claims 1, 10, 19, and 28, Testardi discloses a network, switch fabric, storage processing device, method, comprising:

at least one host adapted to be connected to a switched fabric (hosts 14a-14n connected to fabric 20 shown in figure 3);

at least two storage units, each adapted to be connected to a switched fabric (storage units 22a-22n shown in figure 3).

a switched fabric (switched fabric 20, figure 2) for connection to and coupling of at least one host and at least two storage units (hosts and physical devices shown in figure 2), comprising:

at least one switch for coupling to the at least one host and the at least two storage units (one or more switches discussed in paragraph 62),

a storage processing device (virtualization engines 34a-c, figure 3, details in figures 4A-4C, and later figures) coupled to the at least one switch and for coupling to the at least one host and the first and second storage units of the at least two storage units, where the first and second storage units may be directly connected to the storage processing device or may be coupled through the at least one switch (storage device may be implemented to be part of switch or storage device, paragraph 67), the storage processing device to migrate data between first and second storage units of the at least two storage units whether the first and second storage units are directly connected to the storage processing device or are coupled through the at least one switch (online migration, paragraph 65), the storage processing device comprising:

an input/output module (collection of fast paths processors) for coupling to a first and second storage units (storage units 20a-20n) including processors (fast path processors, “FP”, shown in figure 4A-4C) to receive, operate on, and transmit network traffic (paragraphs 64, 72, 73);

a control module (control path processors, “CP”, shown in figures 4A-4C) coupled to said input/output module, said input/output module and said control module being configured to interactively perform data migration (on-line migration) from the first storage unit to the second storage unit (paragraph 74-75, details of migration discussed in paragraphs 204-212).

Examiner notes that the preambles of claims 1 and 28 appear to be directed to the environment in which the storage processing device/method is used. Therefore, the above rejections are based on the assumption that the preamble limits the claim, and therefore identical in scope to claim 19.

Regarding claim 2, Edsall and Testardi combined disclose claim 1, and Testardi further discloses wherein said processors include table information (figure 23, Rmap 560 and redirect tables) related to data migration (paragraph 204) and wherein said control module is coupled to said table information to maintain said table information for data migration (paragraph 206, 209).

Regarding claim 3, Edsall and Testardi combined disclose claim 2, and Testardi further discloses wherein table information includes a barrier entry (barrier range) and said processors delay data write operations if said barrier entry relates to said data write operation (retried later, paragraph 207).

Regarding claim 4, Edsall and Testardi combined disclose claim 2, and Testardi further discloses wherein said table information includes an entry (entries of tables shown in figure 23) related to the extents in the data migration, said entry defining an extent operation type (paragraph 204, 207).

Regarding claim 5, Edsall and Testardi combined disclose claim 4, and Testardi further discloses wherein said table information further includes a legend entry (rmap) for each extent operation type defining operations for the extent (paragraph 207). Regarding claim 6, Edsall and Testardi combined disclose claim 5, and Testardi further discloses wherein said table information further includes entries referenced by said legend entry defining physical extent location. Examiner notes that the data migration is performed between two physical volumes, and therefore the table information mapping extents in the migration operation reference physical locations of the extents.

Regarding claim 7, Edsall and Testardi combined disclose claim 6, and Testardi further discloses wherein legend entries include entries indicating data not migrated (entry value 1), data migrated (entry value 2), and a barrier entry for data being migrated (barrier range; read-only field 'r/o').

Regarding claim 8, Edsall and Testardi combined disclose claim 7, and Testardi further discloses wherein said processors delay data write operations if said barrier entry relates to said data write operations ("write operation faulted to CP to be later retried", paragraph 207).

Regarding claim 9, Edsall and Testardi combined disclose claim 8, and Testardi further discloses wherein said control module provides commands to copy data and places said barrier entry for said data being copied (paragraph 206).

Regarding claims 11-18, 20-27, and 29-36, examiner notes that these claims are substantially similar to claims 2-9 above. The same grounds of rejection are applied.

(10) Response to Argument

I. Claims 1, 10, 19, 28

Issue I – 112 Rejection

Appellant argued that the rejection is improper because the claim clearly sets up two alternative structures, namely, "the first where the storage units are directly connected to the storage processing device and the second where the storage units are coupled to the storage processing device through at least one switch".

Examiner's Response to the Issue

Applicant's arguments are persuasive and the rejection under 35 U.S.C 112 is withdrawn.

Issue II – 102 Rejection

Appellant argues, in light of the previous arguments regarding the 112 rejection, that prior art, Testardi, does not disclose that "the storage devices can be connected through a switch and have the processing of Testardi still be operational".

Examiner's Response to the Issue

Examiner notes that the two structures are alternatives, then Testardi only needs to show that the processing is functional for the direct connection structure – one of the two alternatives.

However, even assuming that both structures are required, Testardi clearly states that "the data storage system 12 may also include switching fabric 20 which may include one or more switches and other associated hardware and software in connection with facilitating data transmissions between each of the host computer systems and the physical devices" (paragraph 62, example also shown in figure 4C). So Testardi discloses both structures, contrary to appellant's arguments.

II. Claims 3, 12, 17, 21, 26, 30, 35

Issue I – 102 rejection

Appellant argues that the fast path does not delay the operation, but only passes the operation on to the control path.

Examiner's Response to the Issue

Examiner agrees with appellant that the fast path passes the operation on to the control path. However, examiner further notes that fast path makes the decision to pass the operation on to the control path, which is a slower processor system (see, for example, paragraph 74 for a brief explanation of the fast path and control path processors). The fact that the decision is made by the fast path that the operation can only be processed by the control path and subsequently

passing the operation to the control path, the slower processor, clearly indicates that the fast path is at least partly responsible for delaying the operation.

Therefore, appellant's argument that the fast path does not delay the operation is flawed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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